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Nano-Fabrication Techniques for All-Optical Sequential Logic Circuits: A Review

Zahraa Alshannoon[1*] **and Saif Hasan Abdulnabi**[1,2,3]

[1]Department of Electronic and Communications Engineering, Faculty of Engineering, University of Kufa, Najaf, Iraq.

[2]Department of Electrical Engineering, College of Engineering, University of Baghdad, Baghdad, Iraq.

[3]Almakeen Institution for Science and Knowledge, Najaf, Iraq

Corresponding Author: saifh.altameemi@uokufa.edu.iq

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Abstract

To fabricate nanoscale sequential logic circuits, a series of processes to shape, define, and perfect the device geometry must be carefully orchestrated. The aim of this work is to clarify the basic fabrication processes for manufacturing sequences of logic circuits, underscoring actual methodologies in which one can form an exact nanoscale configuration. The process begins with thin-film deposition, including the formation of basic metal or dielectric layers using methods such as physical vapor deposition (PVD) and chemical vapor deposition (CVD). Once the material stack is prepared, circuit geometry is defined by high-resolution patterning techniques, such as e-beam lithography, UV lithography, or nanoimprint lithography. These patterns are then transferred to the deposited films with plasma etchings such as RIE (Reactive Ion Etching) or ICP (Inductively Coupled Plasma) to shape the optical or plasmonic features. In the final stage, state-of-the-art fabrication methods (being, among others, focused ion beam milling, two-photon polymerization, or 3D direct laser writing) are used to fine-tune particular regions or specific complex structures. These combined processes present an easily implemented, versatile fabrication strategy for complex geometries required in plasmonic and photonic sequential logic devices.

Introduction:

Sequential logic is a core component of current photonic and plasmonic systems, in which information processing, as well as state retention, necessitate precisely engineered light-matter interactions. As research trends move toward ultra-compact and high-speed on-chip computing, the fabrication of these circuits has become a decisive factor in determining their performance and reliability. At the nano-scale, small variations of material quality, interface roughness, or patterning accuracy can have a dramatic impact on the optical confinement and switching performance, so that dedicated fabrication techniques are required to guarantee long-lasting device performance [1,2].

The development of photonic and plasmonic logic circuits begins by having a strong material base, which can be achieved through thin-film deposition processes such as physical vapor deposition (PVD) and chemical vapor deposition (CVD). This is incorporated into semiconductor (and nanophotonic) fabrication, as it produces uniform and high-purity layers, which are critical for proper waveguiding and plasmonic excitation [3]. After forming the stack of materials, high-resolution patterning techniques (e.g., electron beam lithography, UV photolithography, and nanoimprint lithography) are applied to define the circuit geometry with precision better than 100 nm [4,5]. The patterned features are then transferred into the underlying films through plasma etching processing, such as reactive-ion etching (RIE) and inductively coupled plasma (ICP) etching. The developed approaches provide a versatile shaping of waveguides, couplers, and resonators, making it possible to design sophisticated photonic structures for advanced applications [6].

For advanced or highly compact plasmonic devices, additional fabrication methodologies, such as FIB milling and direct laser writing, are typically required to fabricate complex 3D (three-dimensional) and/or deeply subwavelength features. Due to their high precision-oriented transfer, these methods have been fundamental in the realization of plasmonic switches, multimode interference logic gates, and nanostructured resonators [7–8]. It is also important to understand the effect of each fabrication process on device performance, since the knowledge has the potential to bridge the gap between theoretical designs and practical sequential circuits. Here, we wish to clarify these fabrication steps and bring out the practical considerations for building nanoscale optical circuits that metrologically operate with high speed and low loss.

In this paper, we provide an overview of the manufacturing process of all-optical sequential logic circuits (AO-SLCs), with the challenges and potential solutions are also addressed. Section 2 describes the fabrication steps for sequential logic circuits in detail. Section 3 concludes and provides references.

Fabrication Techniques Of AO-SLC:

The implementation of all-optical sequential logic circuits (e.g., flip-flops and memory cells) ultimately depends on the availability of accurate nanofabrication techniques that enable the definition of subwavelength features, high-index contrast, and the reliable integration of active and passive components. The particular fabrication process utilized may be highly different from one another, depending on physical mechanisms such as that of photonic crystal resonance, plasmon confinement, or graphene tunability. Each of these options involves specific process control requirements and material compatibility issues. Figure 1: Schematic representation of the necessary fabrication steps in building up nanoscale sequential logic circuits [9].

The process starts with thin-film deposition, where physical vapor deposition (PVD) and chemical vapor deposition (CVD) methods are employed for forming high-quality metal and dielectric layers. Subsequent pattern definition techniques, however, such as electron-beam lithography (EBL), ultraviolet lithography (UV), and nanoimprint lithography (NIL), are used to create complex nanostructures with sub-wavelength resolution. After having defined the patterns, they are transferred into the substrate by means of etching processes such as reactive ION etching (RIE) or inductively coupled plasma (ICP) etching, which guarantees vertical profiles and dimensional accuracy. Lastly, advanced engineering methods such as focused ion beam (FIB) milling, two-photon polymerization (2PP), and 3D direct laser writing are used to generate complex hybrid or 3D geometries. This allows them to create very compact, multifunctional photonic and plasmonic logic elements. Together, these stages represent a flexible set of tools for implementing ultrafast, energy-efficient all-optical circuits.

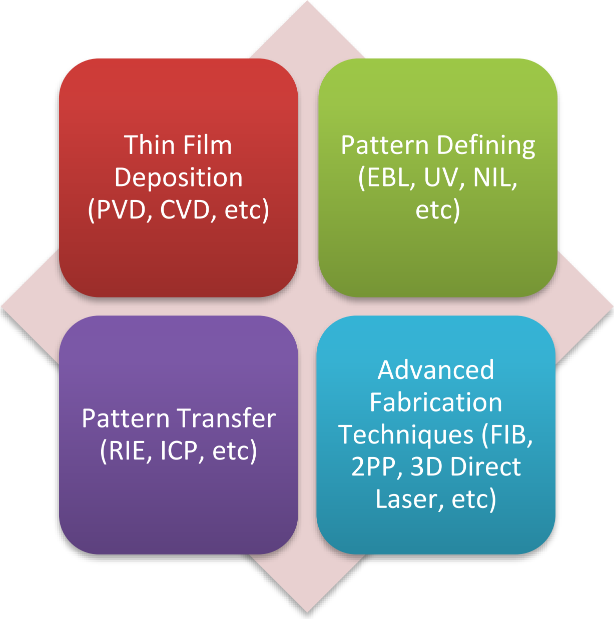

Figure 1: Fabrication steps for sequential logic circuits [9].

1. Thin Film Deposition

The deposition of thin films acts as the most important initial step in the manufacturing of optical logic gates. The metal and dielectric layers deposited in this stage constitute the basic components for plasmonic and photonic nanostructures.

1.1 Physical Vapor Deposition (PVD)

The deposition of metals such as gold (Au), silver (Ag), and aluminum (Al) can be performed using techniques like electron-beam evaporation and sputtering. These two materials enable the excitation of surface plasmon polaritons (SPPs) and make it possible to concentrate light on a plasmonic flip-flop. While PVD can control the thickness and purity of deposit films, achieving an extremely smooth surface is still challenging. Post-deposition annealing is therefore commonly required to promote activation and reduce optical losses [10].

1.2 Chemical Vapor Deposition (CVD)

Dielectric films, often silicon dioxide (SiO_2) or silicon nitride (Si_3N_4), are deposited using plasma-enhanced CVD (PECVD) or atomic layer deposition (ALD). ALD is particularly advantageous for its monolayer-level precision and conformal coating, essential for fabricating photonic crystal cavities and waveguides with controlled resonance properties [11]. For plasmonic logic circuits, which leverage subwavelength field confinement at metal–dielectric interfaces, fabrication is particularly challenging due to the nanoscale alignment required between metal layers and dielectric slots; Figure 2 shows a Profile of a surface plasmon polariton (SPP) on an air-Au interface [12]. These circuits often adopt metal–insulator–metal (MIM) or insulator–metal–insulator (IMI) geometries. In one approach, Magno et al. illustrated the integration of plasmonic components into photonic integrated circuits (PICs) through a multi-step process. This includes metallic layer deposition via sputtering or electron-beam evaporation, Electron Beam Lithography (EBL) patterning of nano-antennas and couplers, dielectric coating through plasma-enhanced chemical vapor deposition (PECVD) or atomic layer deposition (ALD), and chemical-mechanical polishing (CMP) for planarization. The resulting structures allow efficient evanescent or grating-assisted coupling with adjacent dielectric waveguides, enabling flip-flop configurations with minimal footprint and high-speed operation [12].

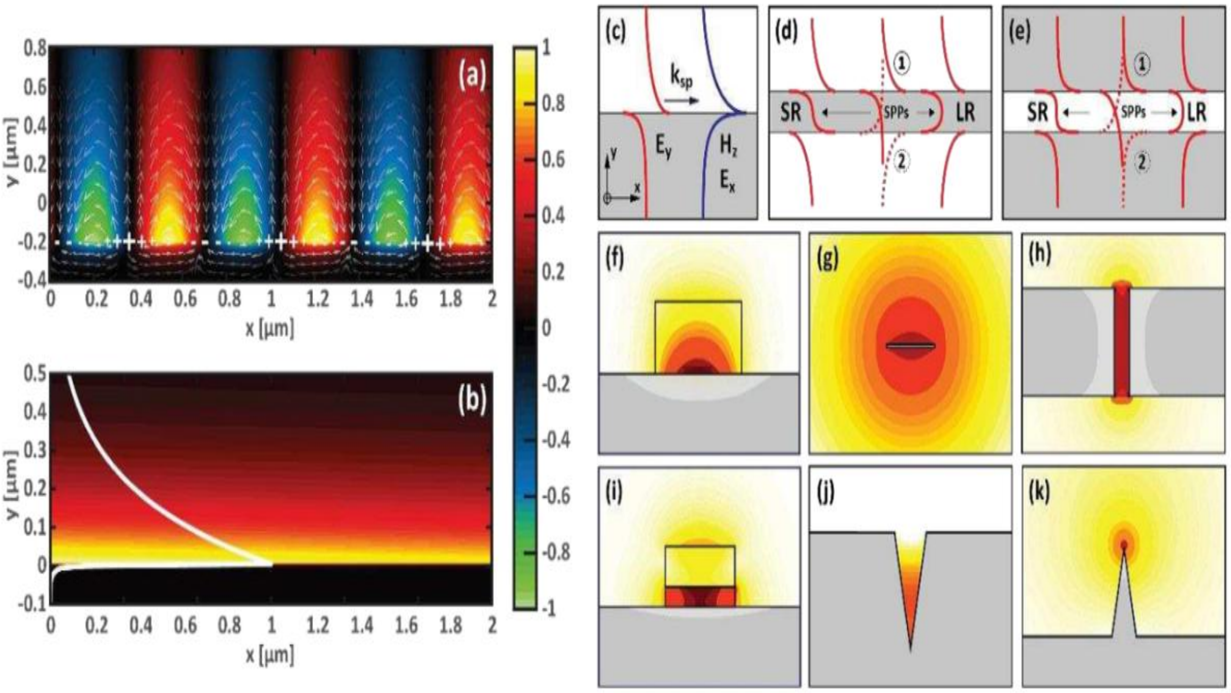

Figure 2: (a,b) Profile of a surface plasmon polariton (SPP) at an air-Au interface, (a) The color scale represents the normalized real part of the x-component of the electric field. (b) The color gradient represents the overall electric field intensity. (c-k) Plasmonic modes are predicted for various waveguide geometries: (c-e) When the electric field propagates along the x-direction, the real part (red) of the y-component is in-plane with respect to the figure plane. (f-k) electric field intensity of the wave during propagation along the z-direction (out-of-plane with respect to the figure plane).[12].

Recent developments in graphene-based plasmonic logic circuits have further advanced integration possibilities for all-optical sequential logic. Bagheri et al. [13] demonstrated a D flip-flop using a graphene-insulator-metal platform, where a graphene layer is sandwiched between SnO_2 dielectric layers and metallic contacts. The fabrication sequence begins with the transfer of CVD-grown graphene onto a substrate, followed by EBL to pattern the waveguide geometry and define metal contacts. Dielectric spacers are deposited using ALD, and lift-off techniques are used to finalize the structure, as shown in Figure 3. The graphene's chemical potential was electrically tuned to modulate the propagation of surface plasmon polaritons (SPPs), achieving logic functionality with an overall footprint below 1 μm^2 and a contrast ratio exceeding 10 dB. This architecture illustrates how active plasmonic elements can be co-integrated into ultra-compact photonic processors.

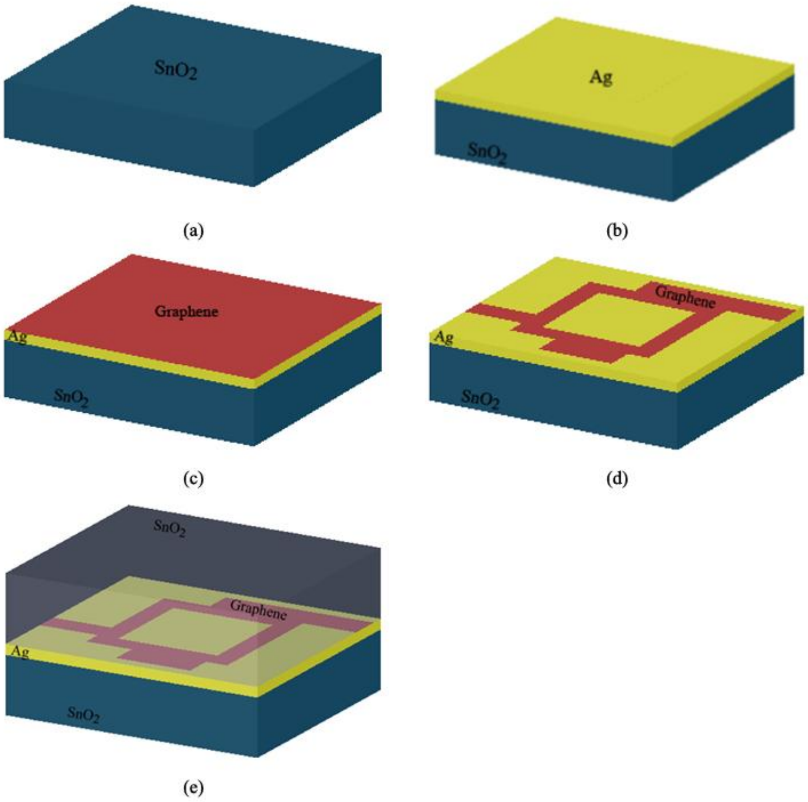

Figure 3: a) SnO_2 substrate grown by mean of chemical vapor deposition (CVD); b) the silver electrode deposited on top of it through electron beam evaporation; c) graphene sheet deposited onto it via CVD method; d) transcribed over the graphene was used as lithographic mask; and e) the resulting scheme allows to form shape-controlled SnO_2 phene sheets [13].

2. Pattern Defining

A high-fidelity definition of nanostructures is important for ultimate performance in sequential logic circuits. Several lithography methods are used to obtain this accuracy.

2.1 Electron Beam Lithography (EBL)

BL is widely used in research because it can achieve a sub-10 nm resolution, enabling the direct patterning of complex structures, such as split-ring resonators and nanorods inserted in plasmonic waveguides. The throughput of EBL is, however, very low, while the cost remains high, making it unsuitable for use in large-scale practical production [14].

2.2 Photolithography or UV Lithography

UV photolithography is widely used in mass production due to its fast processing and mature technology. Combined with the fact that its typical resolution is limited by diffraction to a few tens of nanometers, typically to ~50 nm. To overcome this limitation, further advancements, such as immersion lithography and multiple-patterning techniques, are used for integrating high-density photonic components [15].

2.3 Nanoimprint Lithography (NIL)

NIL is a low-cost, high-throughput process that uses a pre-patterned stamp to generate nanostructures in the resist. This technique has been shown to be efficient for the fabrication of periodic plasmonic arrays and photonic crystals, which are key devices in optical memory cells and flip-flops [16]. In Figure 4, we have depicted the various modes in which nanoscale patterning using NIL can provide insight into memristor operation. Panel I shows atomic force microscopy (AFM) images of a nanoscale crossbar array memristor based on tantalum oxide (TaOx) as the switching material. Comparing the microscale and nanoscale devices reveals that promising material systems can really be scaled down to the few-nm dimension without compromising switching properties. Panel II shows an image of a nano-crossbar array that is structurally preserved after many switching cycles, in contrast to its macro counterparts, where substantial bubbling occurs. This distortion at larger dimensions does not provide good reproducibility, and it is for given cases that the nano-structuration allows for keeping functional properties and thus enhancing both performance and reliability [17].

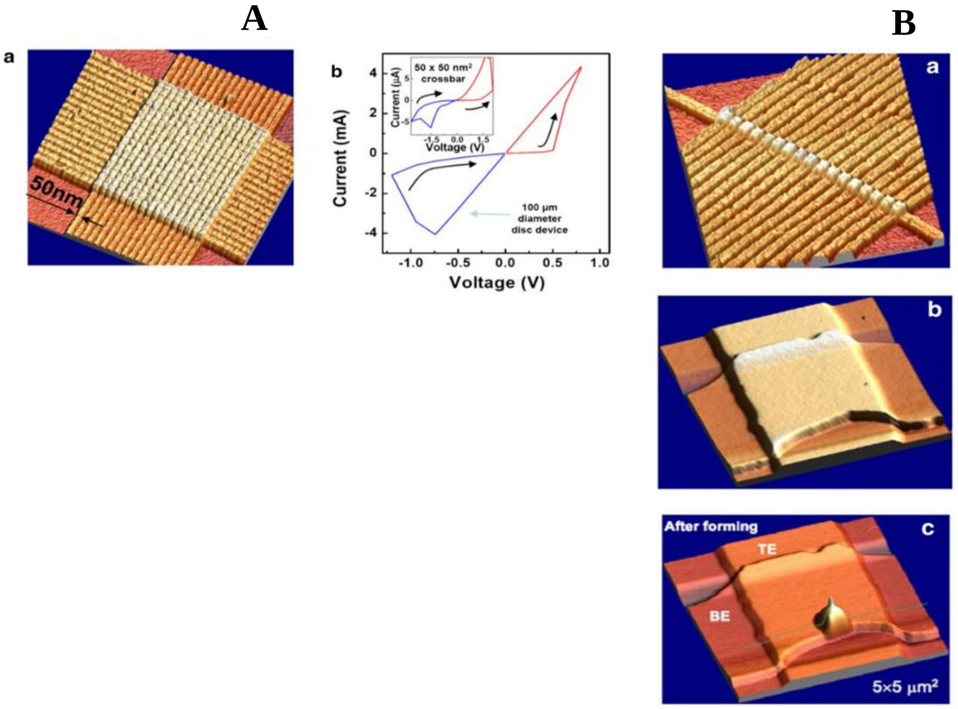

Figure 4: **A)** The switching mechanism of TaOx-based memristive devices was determined using a device array, which included (a) an AFM image of a 50 × 50 nm crossbar array and (b) I-V curves for microscale and nanoscale devices to validate the suggested model [20]. **B)** Nanoscale and microscale memristive devices demonstrate the mechanism of electroforming and ways to mitigate oxygen bubble formation, including AFM images of (a) a nanoscale crossbar array made by nanoimprint lithography and microscale devices (b) before and (c) after electroforming, revealing the formation of a bubble near the filament in the microscale devices only [17].

3. Pattern Transfer

After defining the desired patterns, the next crucial step is to transfer them into the underlying materials with high precision. This is typically achieved through advanced etching techniques. Among these, dry etching methods such as reactive ion etching (RIE) and inductively coupled plasma (ICP) etching which is stand out as the most widely used. These processes have become very popular due to their ability to fabricate fine, high-aspect-ratio features with vertical sidewalls, which is a key requirement for nanostructures like waveguides, photonic crystal lattices, and resonators. Due to dry etching, it plays a crucial role in the fabrication of photonic and plasmonic devices, where relatively small errors impose a dramatic influence on the performance [18].

Furthermore, photonic crystal (PhC)-based memory cells, like the scheme by Pugachov et al. [19], are based on a 2-D square lattice of silicon rods in silica, as the structure shown in Fig. 5. The fabrication followed standard Silicon-on-Insulator (SOI) processes, using electron beam lithography (EBL) and reactive ion etching (RIE) to register the precise position, size, and crystal lattice defects of the rods.

The structures and appearance of these defects have been carefully adjusted to enable two stable resonant states, allowing bistable logic operations. Prior to fabrication, the design was validated extensively through plane wave expansion (PWE) and finite-difference time-domain (FDTD) simulations. These simulations allowed iterative adjustment of the field distributions and switching dynamics, in turn minimizing the requirement for trial-and-error in fabricating a device that would have a reasonable probability of experimental realization.

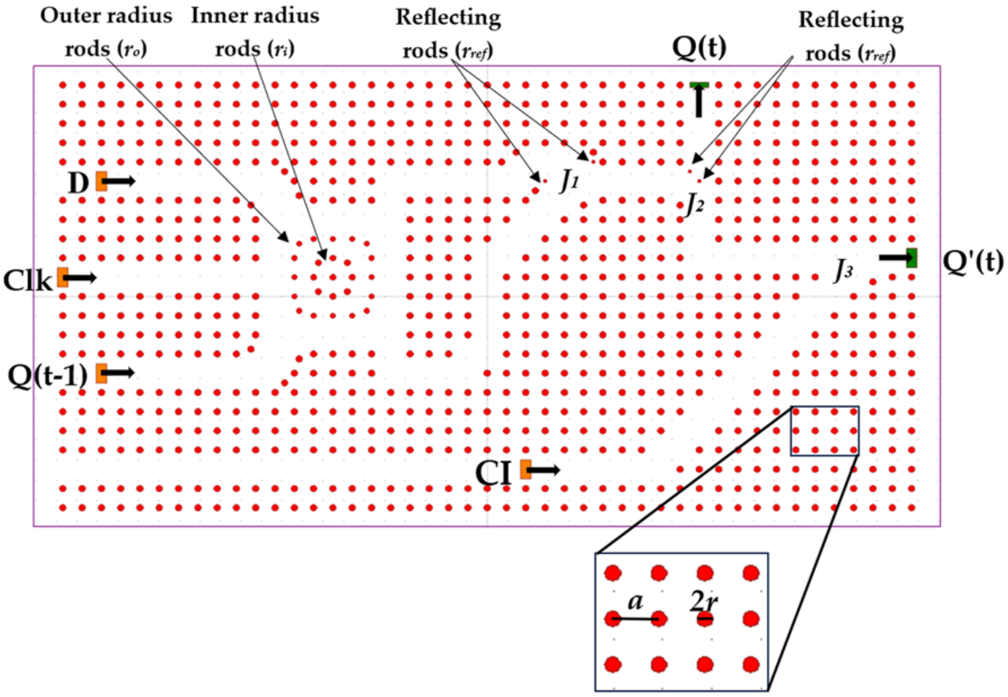

Figure 5: Schematic structure of all-optical D Flip-Flop [19].

4. Advanced Fabrication Techniques

To realize increasingly complex hybrid plasmonic–photonic architectures for sequential logic devices, researchers have turned to cutting-edge fabrication tools.

4.1 Focused Ion Beam (FIB) Milling

FIB enables maskless, direct-write prototyping of nanostructures like plasmonic nano-resonators and photonic crystal cavities. Vesseur et al. demonstrated confined plasmon modes in single-crystal Au resonators created by focused ion beam (FIB) milling [20]. Horák et al. performed a comparative analysis and found that antennas made by the FIB process showed higher surface roughness and contaminants compared to those made using EBL [21], as shown in Figure 6. In addition, an in-depth review highlights the FIB's tremendous potential for high-precision manufacturing of 3D chiral and metal-surface structures [22]. A notable extension of this approach is the use of photonic crystal ring resonators to generate optical feedback and bistability, which are necessary for sequential logic operations. Prather et al. proposed a ring-resonator-based encoder design in Figures 7 and 8. The fabrication process consisted of electron beam lithography (EBL) to define the initial pattern, followed by focused ion beam etching to precisely form the circular defect cavity. This careful treatment allows for smooth edges and high-Q-factor operation by effectively suppressing scatter losses, necessary to maintain bistable logic states in flip-flop designs. The use of FIB, although time-consuming, offers nanometer-scale control that is crucial for sensitive resonator structures embedded within periodic lattices [9].

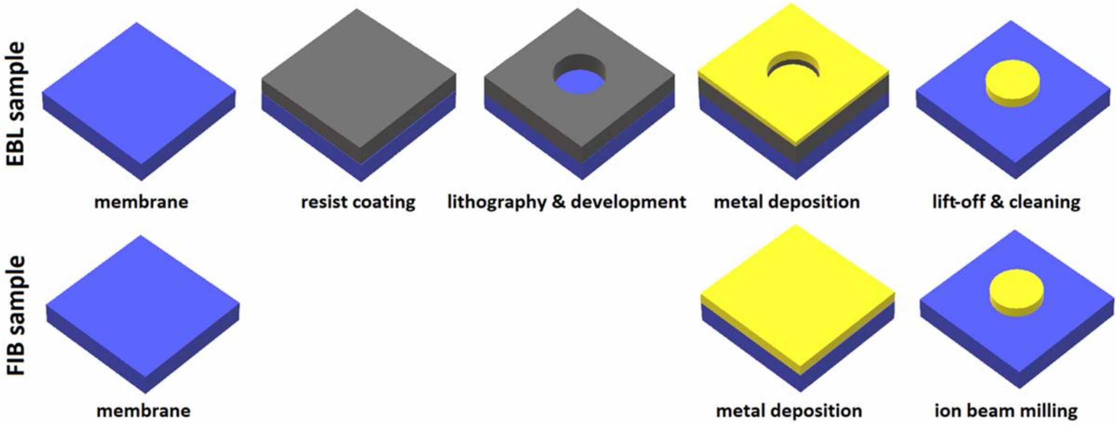

Figure 6: Schematic overview of individual steps in the fabrication process of the EBL and the FIB antennas [21].

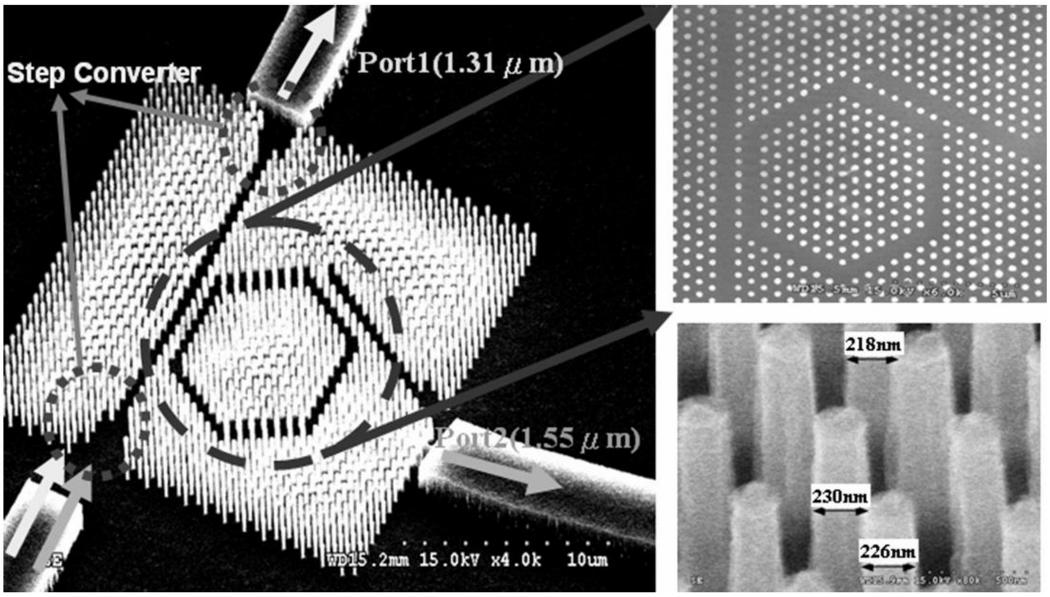

Figure 7: Scanning electron microscopic images of a PhC ring resonator [9, 23].

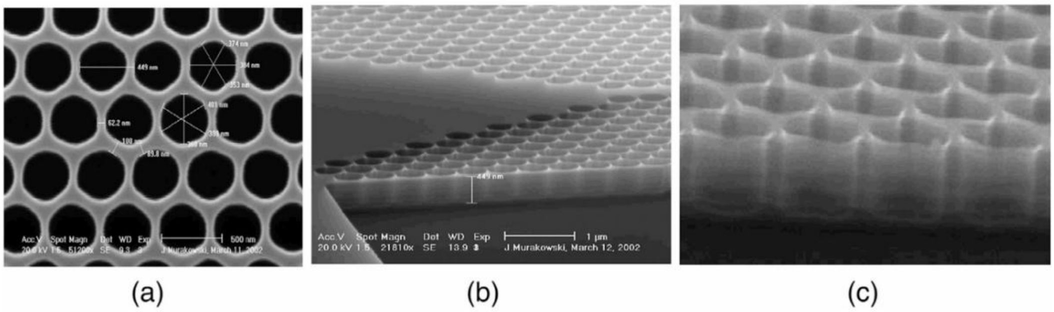

Figure 8: (a) Top-view, (b) perspective view, and (c) zoom-in view of the fabricated PhC device on SOI wafers [9, 24].

4.2 Two-Photon Polymerization (2PP) / Two-Photon Lithography

This direct laser-writing technique enables the fabrication of 3D micro/nanostructures with sub-wavelength precision. Malinauskas et al. outlined their applications for creating micro-resonators in photonic circuits [25]. Additionally, Singhal et al. reported enhanced 3D photonic crystals via sequential infiltration after 2PP, achieving improved refractive index contrast for mid-infrared applications [26].

4.3 3D Direct Laser Writing

With femtosecond lasers, arbitrary 3D geometries are possible, forming the basis for volumetric optical flip-flops, waveguide scaffolds, and reconfigurable circuits [25, 27].

5. Summary of Fabrication Techniques

Overall, the fabrication of all-optical sequential logic circuits requires a combination of high-resolution lithography, material-specific etching or deposition, and multilayer alignment precision. Depending on the chosen architecture, different trade-offs arise in terms of fabrication complexity, compatibility with CMOS back-end processing, and achievable device performance. Table 1 summarizes the fabrication techniques.

Table (2-1) Summary of Key Fabrication Techniques

Fabrication stage	**References**	**Technique**	**Cost**	**Complexity**	**Accuracy**	**Advantages**	**Disadvantages**	**Applications**
Thin Film Deposition	10-13, 28-30	PVD	Moderate	Medium	High	Simple setup and widely available; effective for metal films	Less conformal on high-aspect structures; potential stress in films	Used for depositing metallic layers in plasmonic waveguides and electrodes.
		CVD	Moderate to High	Medium	High	Produces uniform, conformal coatings	Requires high temperatures and stringent process controls	Ideal for dielectric layers in photonic

						even on complex surfaces		crystals and waveguides.
Pattern Defining	14-17, 31-35	EBL	Very High	Very High	Ultra-High	Offers unmatched resolution and flexible patterning for research	Slow and low throughput; not practical for large-scale production	Used in defining nano-antennas, photonic crystal lattices, and defect cavities.
		UV Lithography	Moderate	Medium	Moderate to High	Fast and mature technology for large-area devices	Resolution limited by diffraction; requires enhancements for finer patterns	Standard for mass-producing waveguide circuits and photonic chips.
		NIL	Low to Moderate	Medium	High	Cost-effective for replicating patterns over large areas	Needs high-quality master molds; prone to defect propagation	Used in creating plasmonic arrays and photonic crystal structures.
Pattern Transfer	18, 19, 30, 36-38	RIE	Moderate	Medium to High	High	Enables vertical profiles and precise etching	May cause surface roughness and selectivity issues	Etching of waveguides and photonic crystal cavities.
		ICP	Moderate–High	High	High	Suitable for deep etching and high aspect ratios	Requires advanced equipment and process tuning	Used for fabricating deep photonic crystal cavities.

Advanced Fabrication Techniques	20 – 28, 39, 40	FIB	Very High	Very High	Ultra-High	Allows maskless, site-specific nano-structuring	Slow and costly, with possible Gallium ion damage to sensitive structures	Precise defect engineering in photonic crystals and ring resonators.
		2PP	High	Very High	High	Enables complex 3D micro/nanostructures	Limited to certain resins; time-intensive	Used for micro-resonators and intricate 3D photonic devices.
		3D Direct Laser Writing	High	Very High	High	Supports arbitrary 3D architectures and volumetric designs	Resolution is limited compared to EBL; slower throughput	Suitable for 3D scaffolds and hybrid plasmonic-photonic circuits.

Conclusion:

The fabrication of nanoscale sequential logic circuits depends on a coordinated set of processes that collectively determine the device’s structural accuracy and optical performance. From the thin film deposition stage to the precision patterning and etching steps, which define waveguides and active regions, each process determines how well the circuit is able to guide, confine, and control light. Advanced refining methods, such as FIB milling and direct laser writing, further expand the design freedom to more complex geometries at subwavelength levels that are critical for plasmonic and photonic logic operations. With a full understanding of these fabrication processes and their limitations, scientists can guide theoretical designs to practical fabrication more efficiently so that the sequential logic circuits can meet rigorous requirements of high-speed, sharp switching, low loss, and compact integration. The realization pathway is more than simple manufacturing; it plays a critical role in device design and defines what can be realized, and is not only confined to the current generation, but sets the limits of future generations of nano-photonically implemented logic systems.

Conflict of interest

Authors should disclose in their manuscript any financial or other substantive conflict of interest that might have influenced the presented results or their interpretation.

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